

## **AMENDMENTS TO THE CLAIMS**

1. (Cancelled)

2. (Cancelled)

3. (Currently amended) The variable amplitude voltage regulator according to Claim 2 6 wherein the predetermined frequency of the output signal of the DSP is a fixed frequency above the audible range and the transistor is switched fully on and off in a ratio determined by the adjustable duty ratio (DR) of the output of the DSP.

4. (Original) The variable amplitude voltage regulator according to Claim 3 wherein the demand level control signal (DLS) is defined by the following equation:

$$DLS = [(R1) / (R1+R2) \times (1-DR) \times ACR]$$

where  $R_1$  is the resistance of the transistor and  $R_2$  is the resistance of the resistor connected in parallel with the collector emitter path of the transistor.

5. (Currently amended) The variable amplitude voltage regulator according to Claim ± 6 wherein the demand level control signal (DLS) is defined by the following equation:

$$DLS = [(R1) / (R1+R2) \times (1-DR) \times ACR]$$

where  $R_1$  is the resistance of the transistor and  $R_2$  is the

1                   resistance of the resistor connected in parallel with the collector  
2                   emitter path of the transistor.  
3  
4

5                 6. (new) A variable amplitude voltage regulator for use in a  
6                 power factor correction system including in combination:  
7

8                   a resistor scaling network consisting of at least one  
9                   variable resistor comprising at lease one bi-polar transistor  
10                  having a base, an emitter, and a collector, the collector emitter  
11                  path of which is connected in parallel with a fixed resistance;  
12

13                  a source of rectified alternating current input voltage  
14                  (ACR) coupled to the resistor scaling network;

15                  a voltage error differential amplifier coupled to the ACR  
16                  and to a reference signal to produce a voltage error signal (VES);  
17

18                  a digital signal processing (DSP) circuit;

19                  means coupling the VES to the DSP to produce an output  
20                  signal at a predetermined frequency with an adjustable duty ratio  
21                  (DR);  
22

23                  means coupling the ACR with the collector emitter path of  
24                  the transistor and the output signal from the DSP to the base of  
25                  the transistor to produce a demand level control signal which  
26                  varies as a function of the VES dc level.